CSCI 210: Computer Architecture
Lecture 16: Combinational Logic

Stephen Checkoway
Slides from Cynthia Taylor

CS History: The Traitorous Eight

From left to right: Gordon Moore, C. Sheldon Roberts, Eugene Kleiner, Robert Noyce, Victor Grinich, Julius Blank, Jean Hoerni and Jay Last. Photo by Wayne Miller.

- All worked for William Shockley, inventor of the transistor, at Shockley Semiconductor
- Shockley was paranoid and a terrible manager
- In 1957, the “Traitorous Eight” left to form Fairchild Semiconductor
- All were between 26 and 33 years old when they left
- Fairchild Semiconductor became the leader of the industry, and was involved in the creation of many other companies, including Intel and AMD

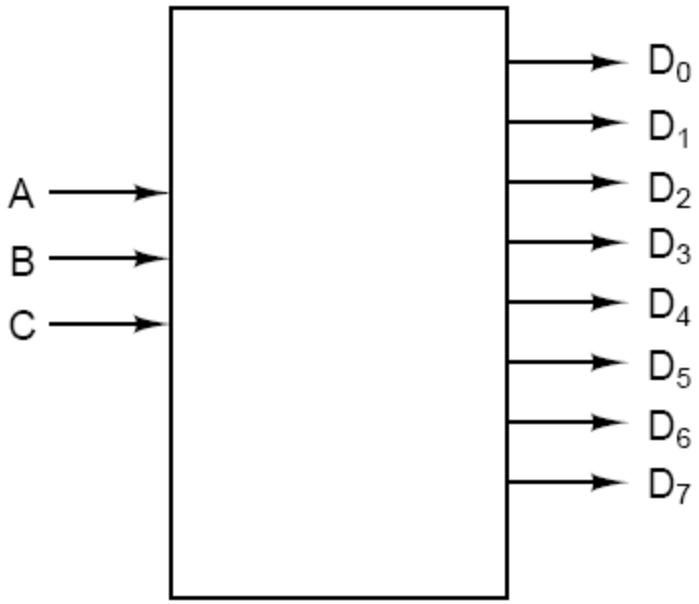
Digital Logic

- Previously: Established rules of Boolean algebra and digital logic

- Today: Building stuff!

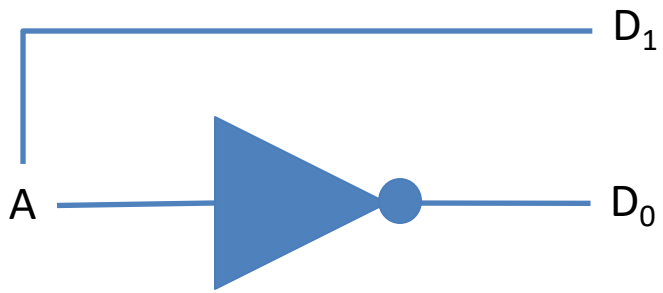
Decoder

- Interprets n inputs (e.g., A, B, C) as an n-bit binary number
- Sets output D_n to 1, all other outputs to 0
- The output is “one hot”



3-to-8 decoder

Creating a Decoder

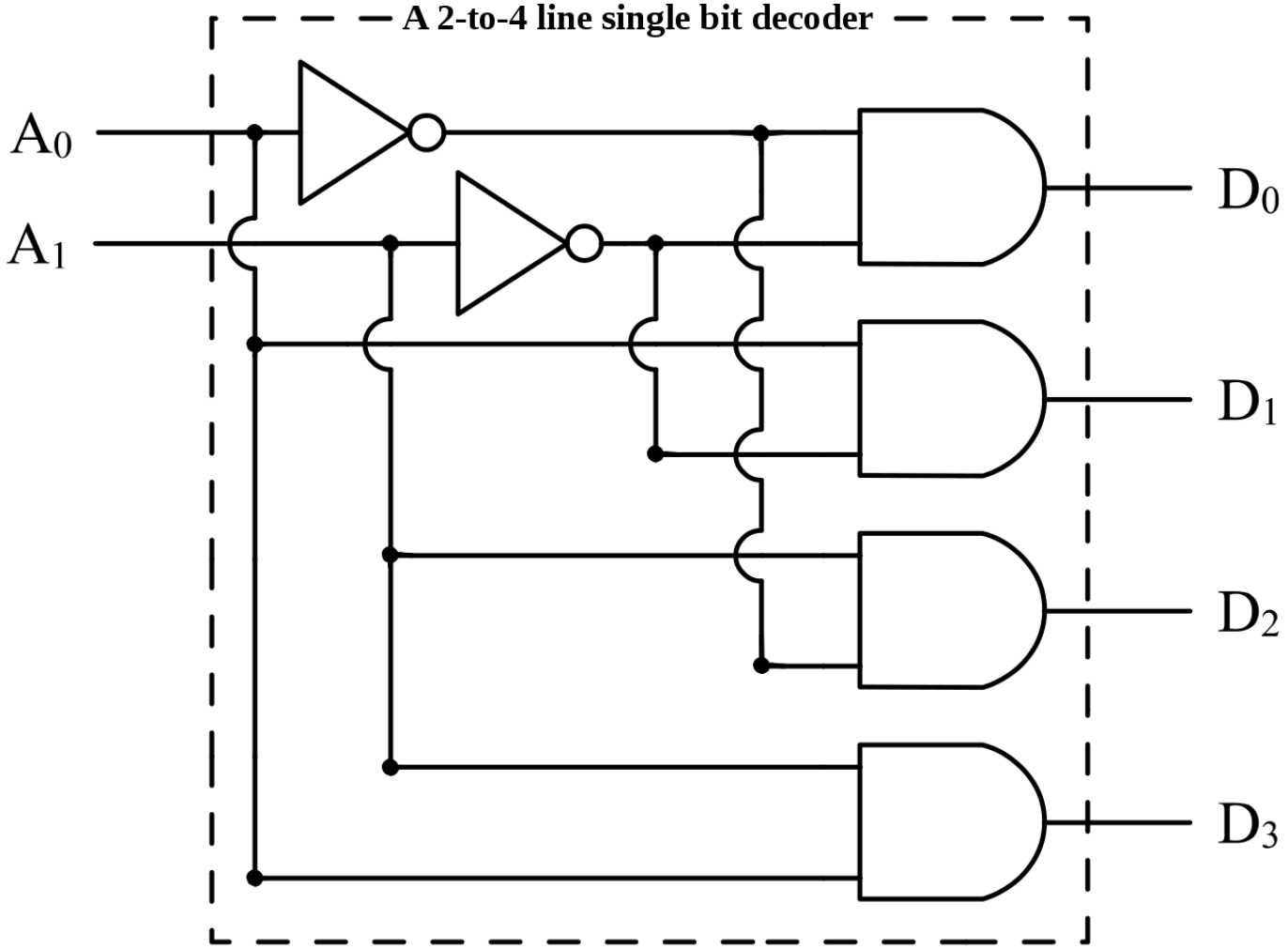


- For each input signal, we need the signal and its complement

- Signals are connected to outputs via AND gates so that inputs turn on only the output that the input represents (e.g., an input value of 5 = 101_2 turns on output D_5

2-to-4 Decoder

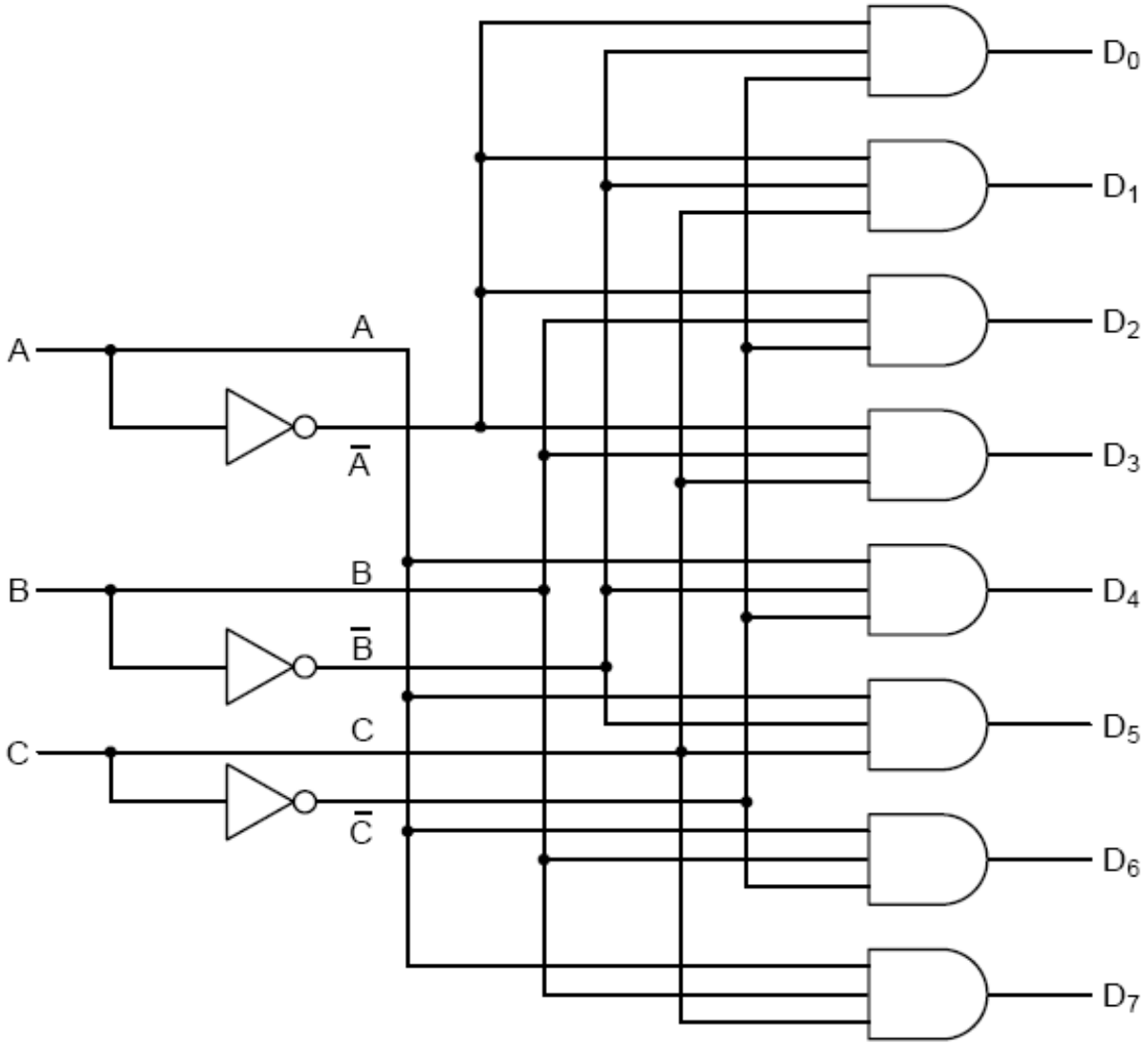
2-to-4 Decoder



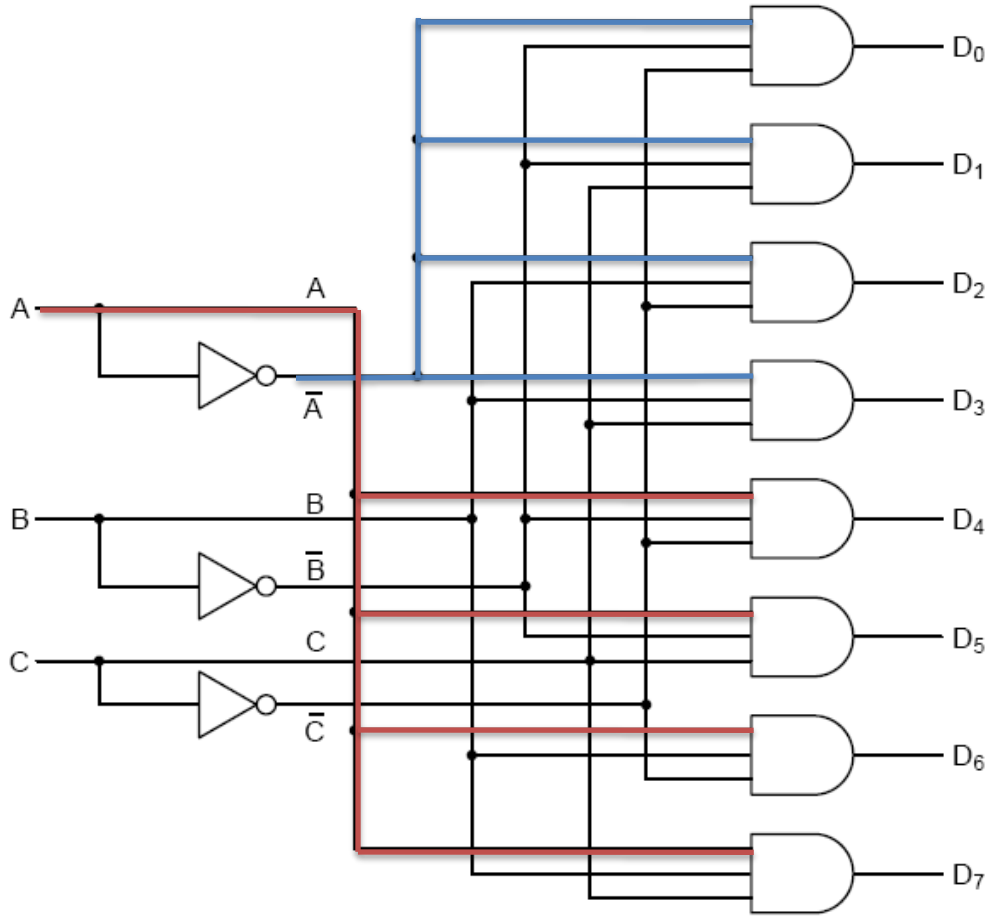
Truth Table

A_1	A_0	D_3	D_2	D_1	D_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

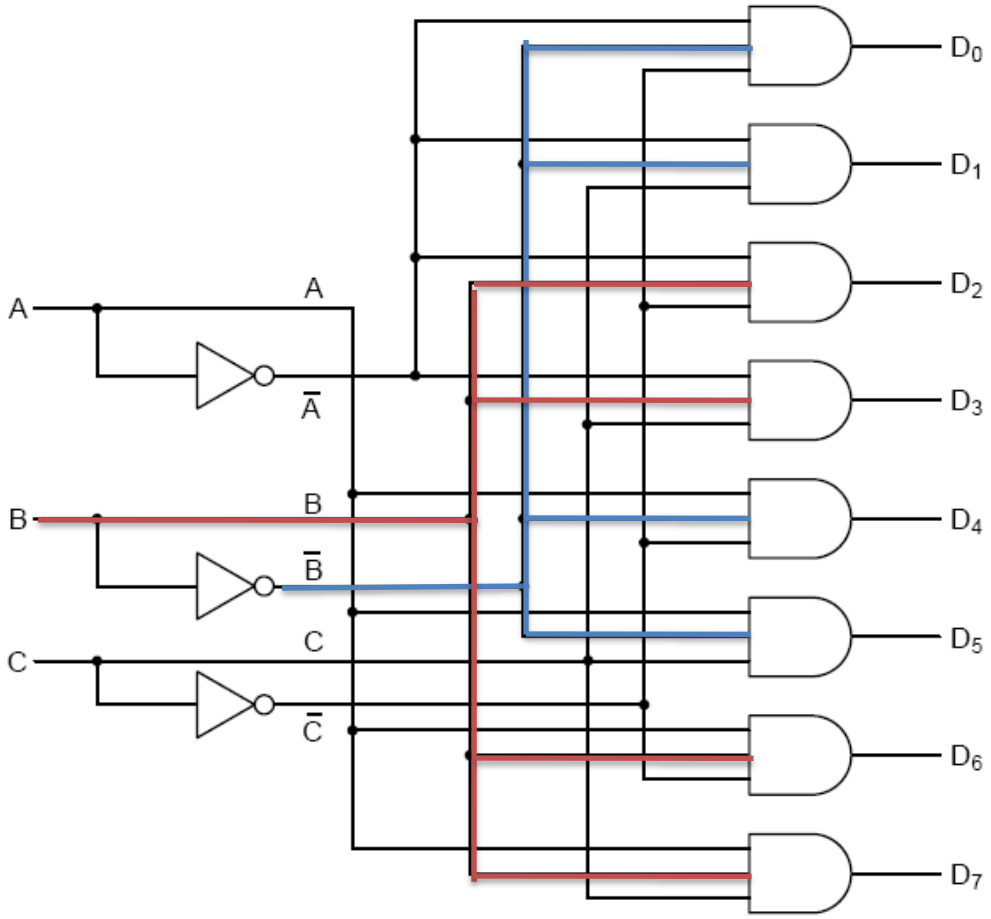
3-to-8 Decoder



3-to-8 Decoder, A is our MSB

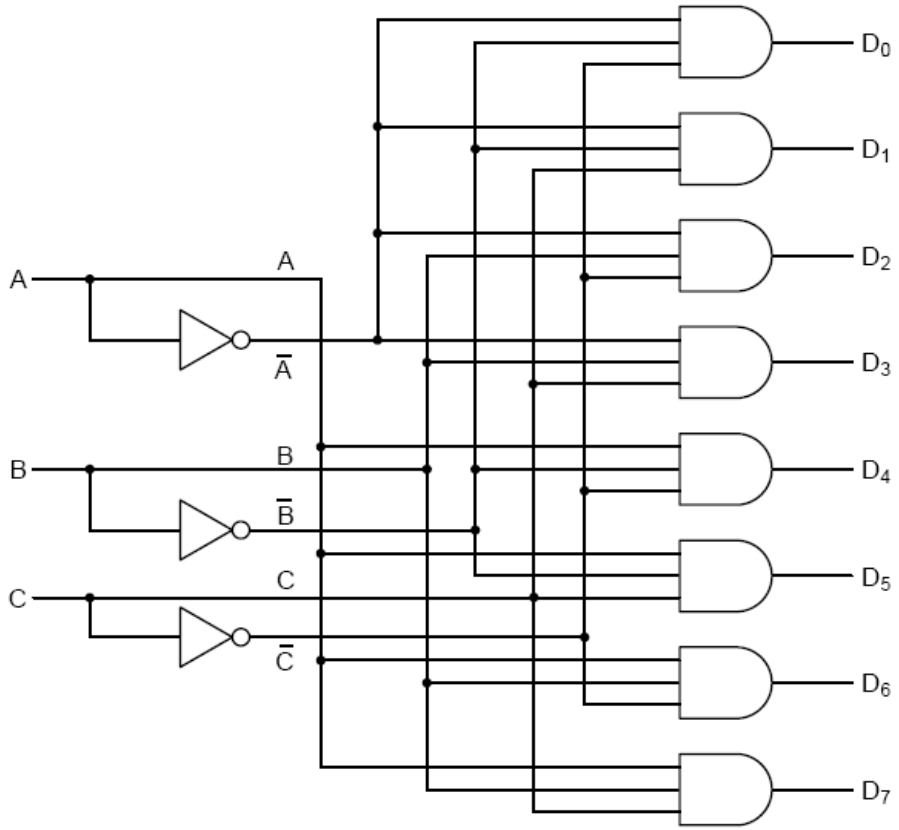


3-to-8 Decoder, B

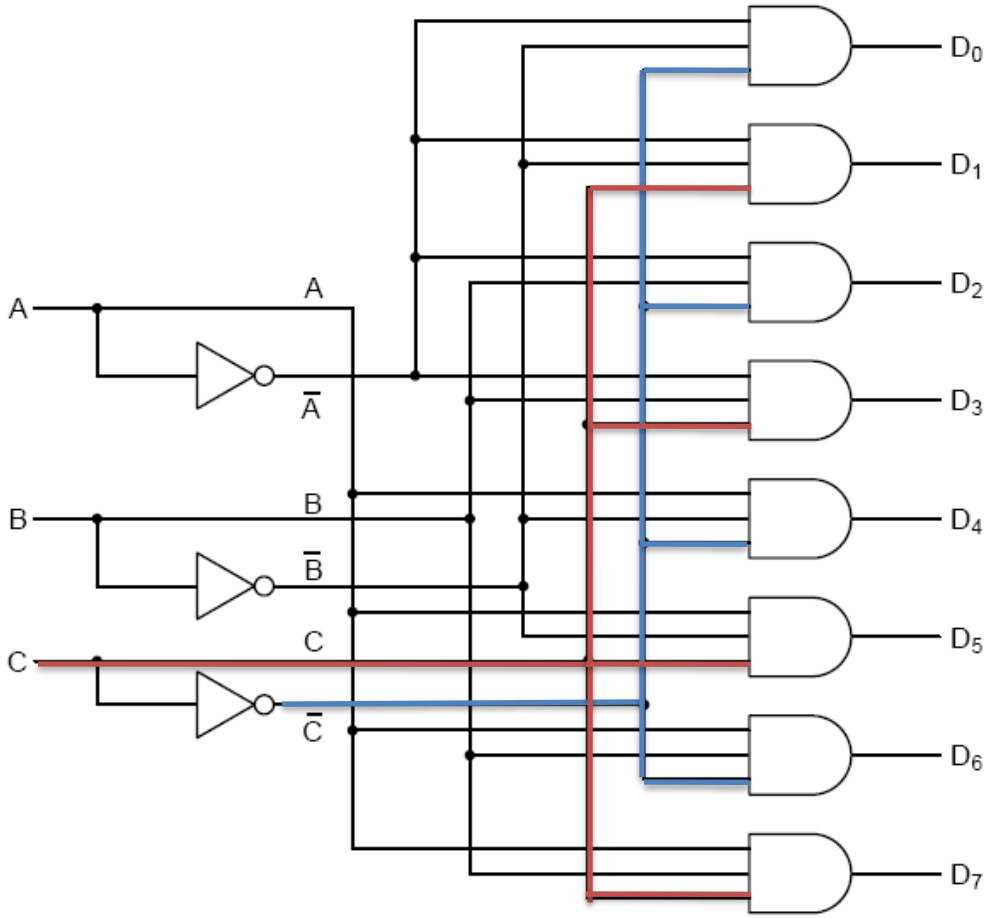


C corresponds to the lowest order bit for the input. In our 3-bit decoder, if C is 1, it sends 0 to _ and 1 to _

Clicker	0	1
A	D0, D1, D2, D3	D4, D5, D6, D7
B	D4, D5, D6, D7	D0, D1, D2, D3
C	D0, D2, D4, D6	D1, D3, D5, D7
D	D1, D3, D5, D7	D0, D2, D4, D6

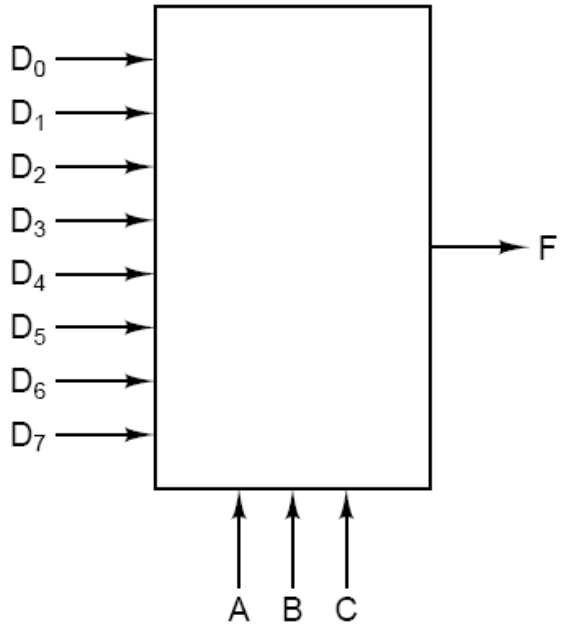


3-8 Decoder, C



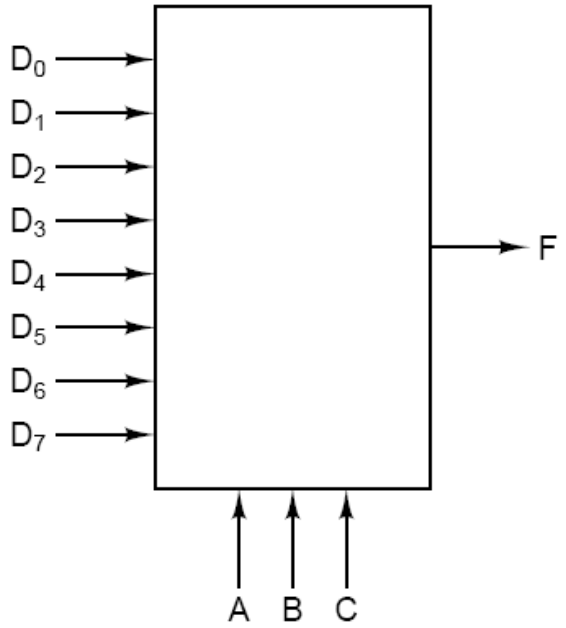
Multiplexer

- Select one signal from a group of 2^n inputs, to be output on a single output line.



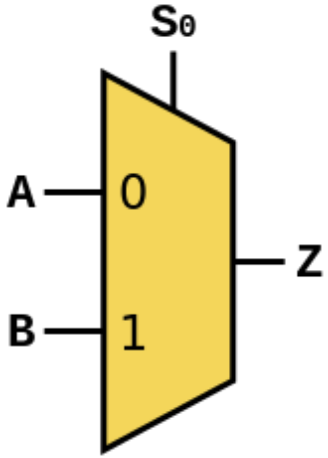
Multiplexer

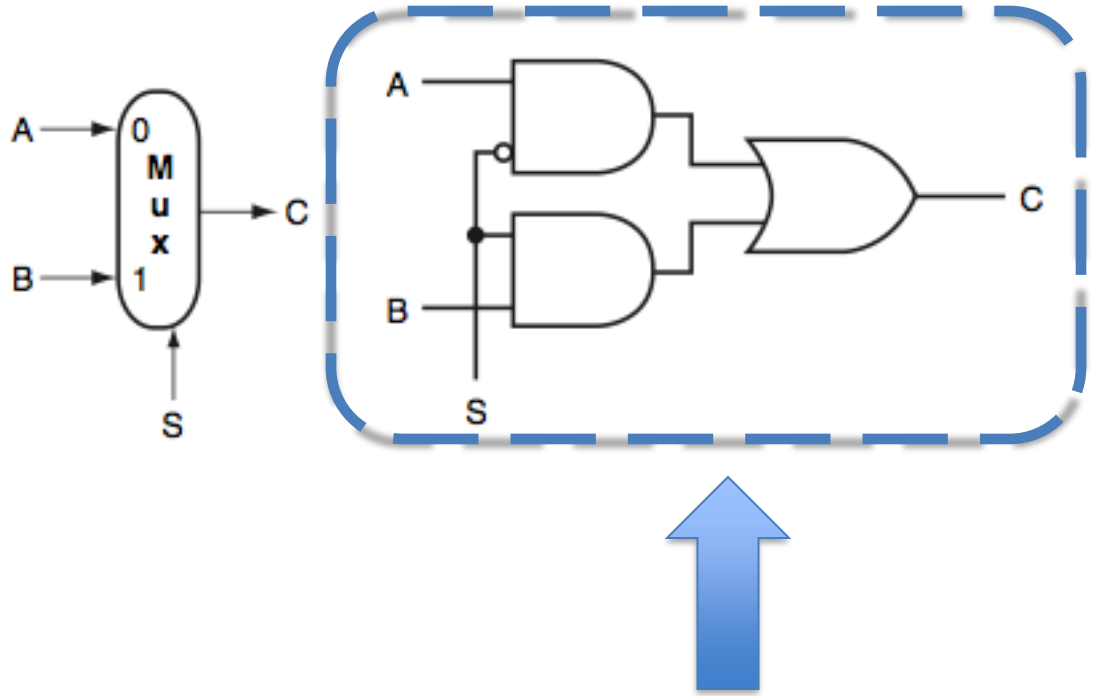
- Lines $D_0,\ldots,D_7$ are the data input lines and F is the output line.
- Lines A, B, and C are called the select lines. They are interpreted as a three-bit binary number, which is used to choose one of the D lines to be output on line F.



2-to-1 Multiplexer

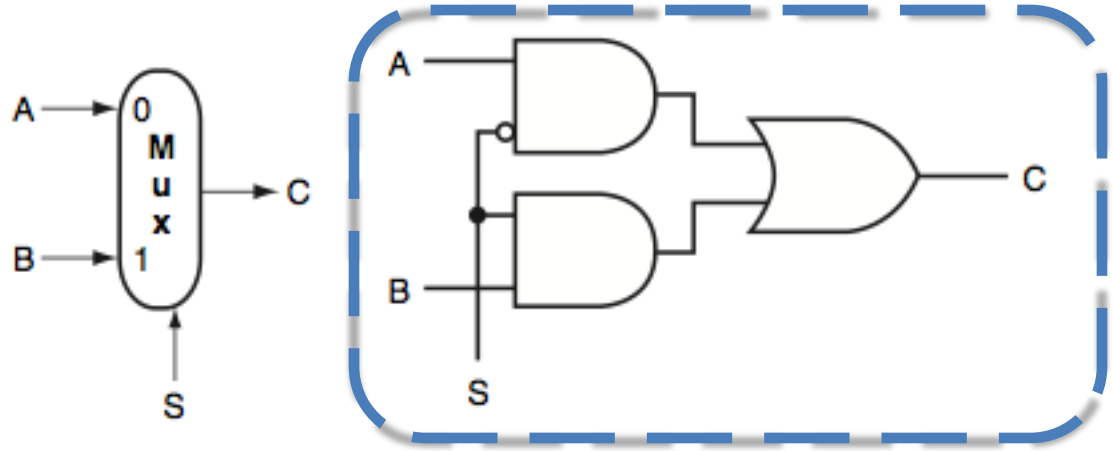
- S is the selector
- 0 selects A; 1 selects B
- Common circuit symbol





Implementation

A = 1, B = 0, and S is 1. C will be



A. 1

B. 0

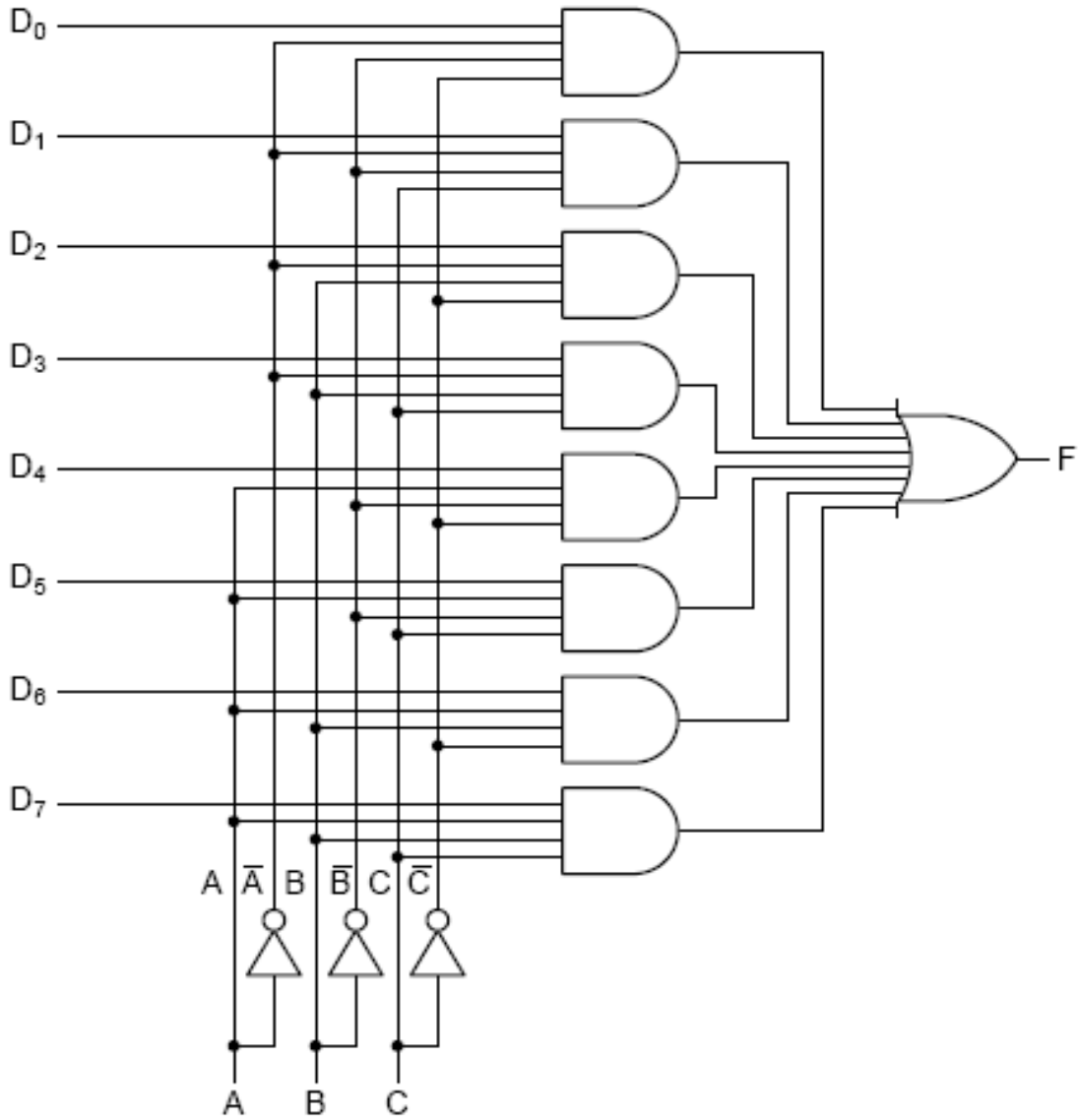
C. Unclear

Arbitrarily Large Multiplexer

- If there are n data inputs, there will need to be $\lceil \log_2 n \rceil$ selector inputs.

- The multiplexer consists of
  - A decoder that generates n signals, each indicating a different control value
  - An array of n AND gates, each combining one of the inputs with a signal from the decoder
  - A single large OR gate that incorporates the outputs of the AND gates

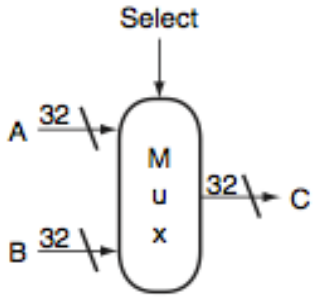
8-to-1 multiplexer



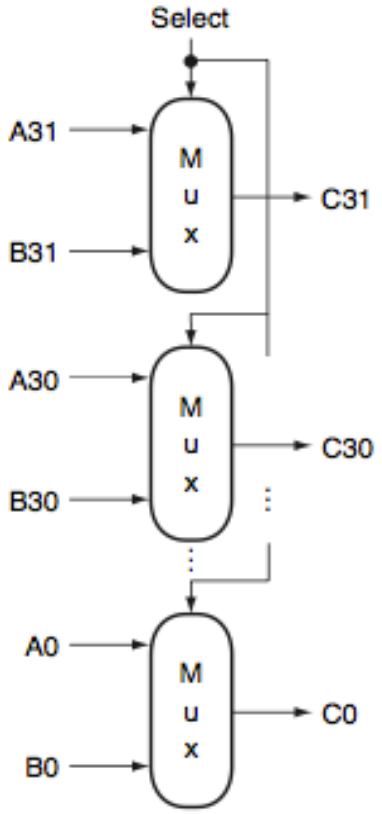
Scaling Up

- Have to perform combinational operations over an entire word (32-bits) of input.
- Bus: a collection of data lines that is treated together as a single logical signal.
- Example: A multiplexer is used to choose which of the two buses (each 32 bits wide) will be written into the Result register

Replicating a 1-bit Multiplexer 32 times



a. A 32-bit wide 2-to-1 multiplexor

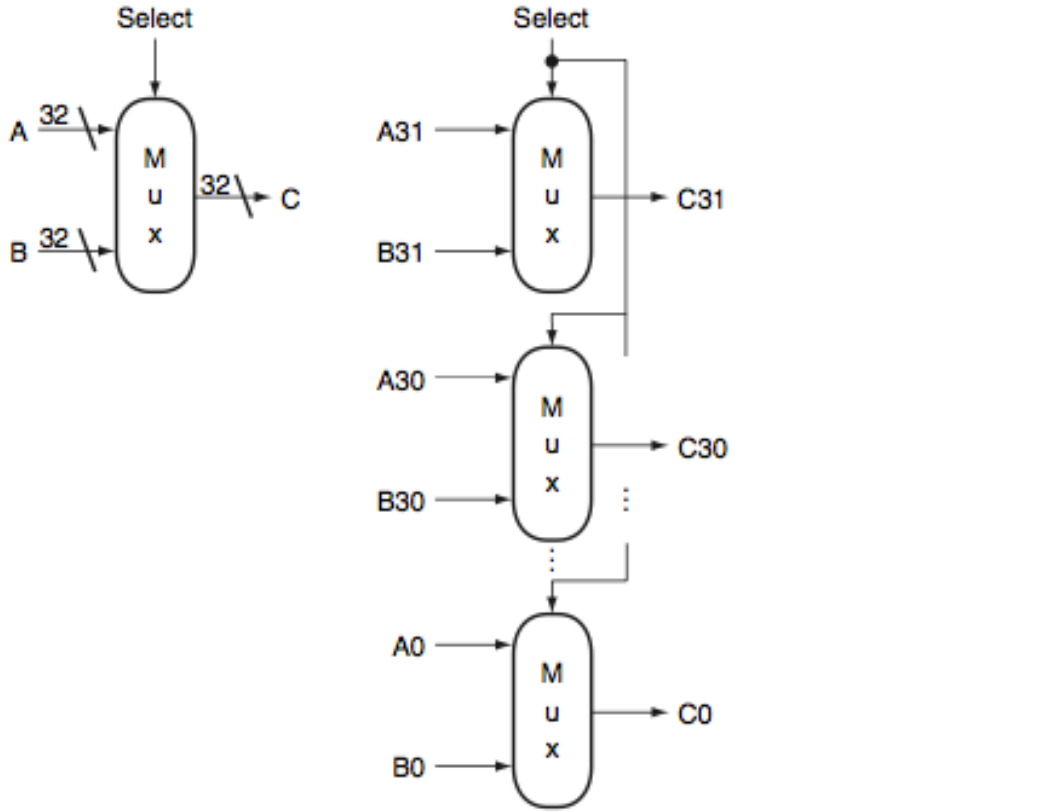


b. The 32-bit wide multiplexor is actually an array of 32 1-bit multiplexors

Will the Select value be the same for each mux?

A. Yes

B. No



a. A 32-bit wide 2-to-1 multiplexor

b. The 32-bit wide multiplexor is actually an array of 32 1-bit multiplexors